WHAT WE CLAIM IS:

1. A semiconductor memory device comprising:

a first and second bit line;

a first word line; and

a memory cell having a first inverter including a first N-channel MOS transistor and a first P-channel MOS transistor, a second inverter including a second N-channel MOS transistor and a second P-channel MOS transistor with an input terminal being coupled to an output terminal of said first inverter and with an output terminal being coupled to an input terminal of said first inverter, a third N-channel MOS transistor having a source/drain path coupled between the output terminal of said first inverter and the first bit line, and a fourth N-channel MOS transistor having a source/drain path coupled between the output terminal of said second inverter and the second bit line;

wherein said first and third N-channel MOS transistors are formed in a first P-type well region,

wherein said second and fourth N-channel MOS transistors are formed in a second P-type well region,

wherein said first and second P-channel MOS transistors are formed in an N-type well region which lies between first and second P-type well region, and

wherein the first P-type well region includes a diffusion layer, wherein an outer shape of the diffusion layer, defined by an isolation layer which extends along the entirety of each of the longitudinal sides of the diffusion layer, is substantially linearly symmetric relative to a line extending in a first direction through said P-type well region, and wherein the boundary of said first P-type well region and said N-type well region extends in said first direction.

2. A semiconductor memory device according to claim 1:

wherein said outer shape of the diffusion layer in the first P-type well is a rectangle.

3. A semiconductor memory device according to claim 1:

wherein said outer shape of the diffusion layer in the first P-type well is an outer shape of a combination of rectangles.

4. A semiconductor memory device according to claim 1:

wherein said first bit line lies between a first power supply line and a first ground line, and

wherein said second bit line lies between said first power supply line and a second ground line, and

wherein said first ground line is coupled to the source of said first N-channel MOS transistor and said second ground line is coupled to the source of said second N-channel MOS transistor.

5. A semiconductor memory device according to claim 4,

wherein said first bit line, said first power supply line, and said first and second ground lines are formed metal layers having the same level at the same metalization level.

6. A semiconductor memory device according to claim 1, wherein the width of the gate of the first N-channel MOS transistor is larger than the width of the gate of the third N-channel MOS transistor.

7. A semiconductor memory device according to claim 1, wherein said first word line lies in a metalization level between the substrate and the first and second bit lines.

8. A semiconductor memory device comprising:

a first, second, third and fourth bit lines;

a first word line; and

a first memory cell having a first inverter including a first N-channel MOS transistor and a first P-channel MOS transistor, a second inverter including a second N-channel MOS transistor and a second P-channel MOS transistor with an input terminal being coupled to an output terminal of said first inverter and with an output terminal being coupled to an input terminal of said first inverter, a third N-channel MOS transistor having a source/drain path coupled between the output terminal of said first inverter and said first bit line, and a fourth N-channel MOS transistor having a source/drain path coupled between the output terminal of said second inverter and said second bit line;

a second memory cell having a third inverter including a fifth N-channel MOS transistor and a third P-channel MOS transistor, a fourth inverter including a sixth N-channel MOS transistor and a fourth P-channel MOS transistor with an input terminal being coupled to an output terminal of said third inverter and with an output terminal being coupled to an input terminal of said third inverter, a seventh N-channel MOS transistor having a source/drain path coupled between the output terminal of said third inverter and said third bit line, and a eighth N-channel MOS transistor having a source/drain path coupled between the output terminal of said fourth inverter and said fourth bit line;

wherein said first, third, fifth, and seventh N-channel transistors are formed in a first P-type well region,

wherein said second and fourth N-channel MOS transistors are formed in a second P-type well region,

wherein said first and second P-channel MOS transistors are formed in a first N-type well region which lies between first and second P-type well regions,

wherein said sixth and eighth N-channel MOS transistors are formed in a third P-type well region,

wherein said third and fourth P-channel MOS transistors are formed in a second N-type well region which lies between first and third P-type well regions, and

wherein a first active region includes the source and drain regions of said first and third N-channel MOS transistors and a second active region includes the source and drain regions of said fifth and seventh N-channel MOS transistors, wherein said first and second active regions are isolated from each other by an isolation layer.

9. The semiconductor memory device according to claim 8,

wherein said isolation layer is SGI.

10. The semiconductor memory device according to claim 8,

wherein said third, fourth, seventh, and eighth N-channel MOS transistors are coupled to said first word line,

wherein the source of said first and fifth N-channel MOS transistors are coupled to each other via first wiring line feeding a first operation potential, and

wherein said first wiring line is formed on the same metalization level of said a first, second, third and fourth bit lines.

11. The semiconductor memory device according to claim 10,

wherein the source of said first and second P-channel MOS transistors are coupled to each other via second wiring line feeding a second operation potential,

wherein said second wiring line is formed on the same metalization level of said a first wiring line, and

wherein said first bit line is laid between said first and second wiring line.

12. The semiconductor memory device according to claim 8,

wherein the gate width of said first N-channel MOS transistor is larger than the gate width of said third N-channel MOS transistor.

13. The semiconductor memory device according to claim 12,

wherein the outershape of the first active region in the first P-type well is substantially linearly symmetric relative to a line in said first P-type well extending in a first direction,

wherein the outershape of the second active region in the second P-type well is substantially linearly symmetric relative to a line in said second P-type well extending in said first direction, and

wherein the boundary of said first P-type well region and N-type well region extends in said first direction.

14. A semiconductor memory device according to claim 1, wherein a first polycrystalline silicon lead layer for use as the gate of said third N-channel MOS transistor and a second polycrystalline silicon lead layer for use as the gate of said first P-channel MOS transistor and also as the gate of said first N-channel MOS

transistor are disposed in parallel to each other, wherein a third polycrystalline silicon lead layer for use as the gate of said fourth N-channel MOS transistor and a fourth polycrystalline silicon lead layer for use as the gate of said second N-channel MOS transistor and also as the gate of said second P-channel MOS transistor are disposed in parallel to each other, and wherein the first and third polycrystalline silicon lead layers are connected via a contact to a second layer of a metal lead layer constituting said first word line.

15. A semiconductor memory device according to claim 1, wherein the input terminal of said first inverter and the output terminal of said second inverter are electrically connected together at a contact whereas the input terminal of said second inverter and the output terminal of said first inverter are electrically connected together at a contact.

16. A semiconductor device comprising first and second inverters with an output of each inverter being as an input of a remaining inverter, a first switch connected to a connection node between an output of the first inverter and an input of the second inverter, and a second switch connected to a connection node between an input of said first inverter and an output of said second inverter,

wherein said semiconductor device has an N-type well region and first and second P-type well regions as disposed on opposite sides of said N-type well region,

a diffusion layer formed in each of said N-type well region and said first and second P-type well regions is arranged in planar shape to have one of (1) a shape consisting essentially of a single rectangle having long sides in an elongate direction of a boundary line of said N-type well region and said first and second P-type well

regions and (2) a shape resulting from combination of a plurality of rectangles in the elongate direction of the boundary line of said N-type well region and said first and second P-well regions, the rectangles having long sides in said elongate direction.

17. A semiconductor device according to claim 16, wherein the diffusion layer formed in said N-type well region and P-type regions has its planar shape resembling a single rectangle having long sides in the elongate direction of boundary lines of said N-type well region and said first and second P-type well regions.

18. A semiconductor device according to claim 16, wherein the diffusion layer formed in said N-type well region or P-type region has its planar shape of a combined form as resulting from combination of a first rectangle having long sides in the elongate direction of boundary lines of said N-type well region and said first and second P-type well regions along with a short side of a first length and a second rectangle having long sides in the elongate direction of the boundary lines of said N-type well region and said first and second P-type well regions along with a short side of a second length, the combination being in the elongate direction of said boundary lines.